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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,013	01/16/2002	Wolfgang Rosner	L&L-I0232	5714

7590 11/10/2003
LERNER AND GREENBERG, P.A.
Post office Box 2480
Hollywood, FL 33022-2480

EXAMINER

ERDEM, FAZLI

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

MSV

Office Action Summary	Application N .	Applicant(s)	
	10/047,013	ROSNER ET A	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 1-9 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 10-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s) _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 10, 11, and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al. (6,498,065) in view of Fitch et al. (5,554,870) further in view of Burns, Jr. et al. (6,077,745).

Regarding Claims 10, 11, and 16, Forbes et al. disclose a memory address decode array with vertical transistors where a decoder for a memory device is provided. The decoder array includes a number of address lines and a number of output lines. The address lines and the output lines form an array. A number of vertical transistors are selectively disposed at intersections of output lines and address lines. Each transistor is formed in at least one pillar of semiconductor material that extends outwardly from a working surface of a substrate. The vertical transistors each include source, drain, and body regions. A gate is also formed along at least one side of the at least one pillar and is coupled to one of the number of address lines. The transistors in the array implement a logic function that selects an output line responsive to an address provided to the address lines. Forbes et al. fail to disclose the required capping layer and insulators and the pillar in the required manner. However, Fitch et al. disclose an integrated circuit having both vertical and horizontal devices and process for making the same where the required capping layer is disclosed. Furthermore, Burns, Jr. et al. disclose a self-aligned diffused

source vertical transistors with stack capacitors in a 4F-Square memory cell array where the required insulators and pillars in the required manner is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required capping layer and the insulator and pillar in the required manner as taught by Fitch et al. and Burns, Jr. et al. respectively in order to have a vertical memory structure with better performance.

2. Claims 12 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al. (6,498,065) in view of Fitch et al. (5,554,870) further in view of Burns, Jr. et al. (6,077,745) further in view of Forbes et al. (6,134,175).

Regarding Claims 12 and 13, Forbes et al., Fitch et al. and Burns, Jr. et al. combination fail to disclose the required doping structure. However, Forbes et al. (6,134,175) disclose a memory address decode array with vertical transistors where the required doping structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required doping structure in Forbes et al. (6,498,065), Fitch et al. and Burns, Jr. et al. as taught by Forbes et al. (6,134,175) in order to have a vertical memory structure with better performance.

3. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al. (6,498,065) in view of Fitch et al. (5,554,870) further in view of Burns, Jr. et al. (6,077,745) further in view of Bertin et al. (6,060,746).

Regarding Claim 14, Forbes et al., Fitch et al. and Burns, Jr. et al. combination fail to disclose the required tunnel structure. However, Bertin et al. disclose a power transistor having vertical FETs and method of making same where the required tunnel structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required tunnel structure in Forbes et al., Fitch et al. and Burns, Jr. et al. as taught by Bertin et al. (6,060,746) in order to have a vertical memory structure with better performance.

4. Claim 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al. (6,498,065) in view of Fitch et al. (5,554,870) further in view of Burns, Jr. et al. (6,077,745) further in view of Biegelsen et al. (5,607,876).

Regarding Claim 15, Forbes et al., Fitch et al. and Burns, Jr. et al. combination fail to disclose the required core structure. However, Biegelsen et al. disclose a fabrication of quantum confinement semiconductor light-emitting device where the required core structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required core structure in Forbes et al., Fitch et al. and Burns, Jr. et al. as taught by Biegelsen et al. (5,607,876) in order to have a vertical memory structure with better performance.

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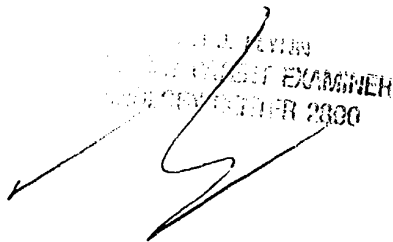
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE
November 2, 2003


NATHAN FLYNN
SUPERVISOR EXAMINER
NOV 02 2003